Standard Products

UT700-LEAP-MEZ
LEAP
Leon Expandable Application Platform

LEAP Board Stack User Guide
August 5, 2015
www.aeroflex.com/LEON

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1.0 Introduction

1.1 Scope

This document describes the Leon Expandable Application Platform (LEAP) design implemented for the Aeroflex UT700 LEON3-FT processor. The LEAP card design is intended to be a low-cost development platform to familiarize users with the Aeroflex UT700 processor, as well as allow custom expansion based on application requirements.

The following hardware and software components are required in order to use the LEAP evaluation board:

- PC work station running Windows XP PRO, Windows 7 or Linux
- Aeroflex Gaisler GRMON-Pro

For new users to UT700 software development, the following tools are recommended:

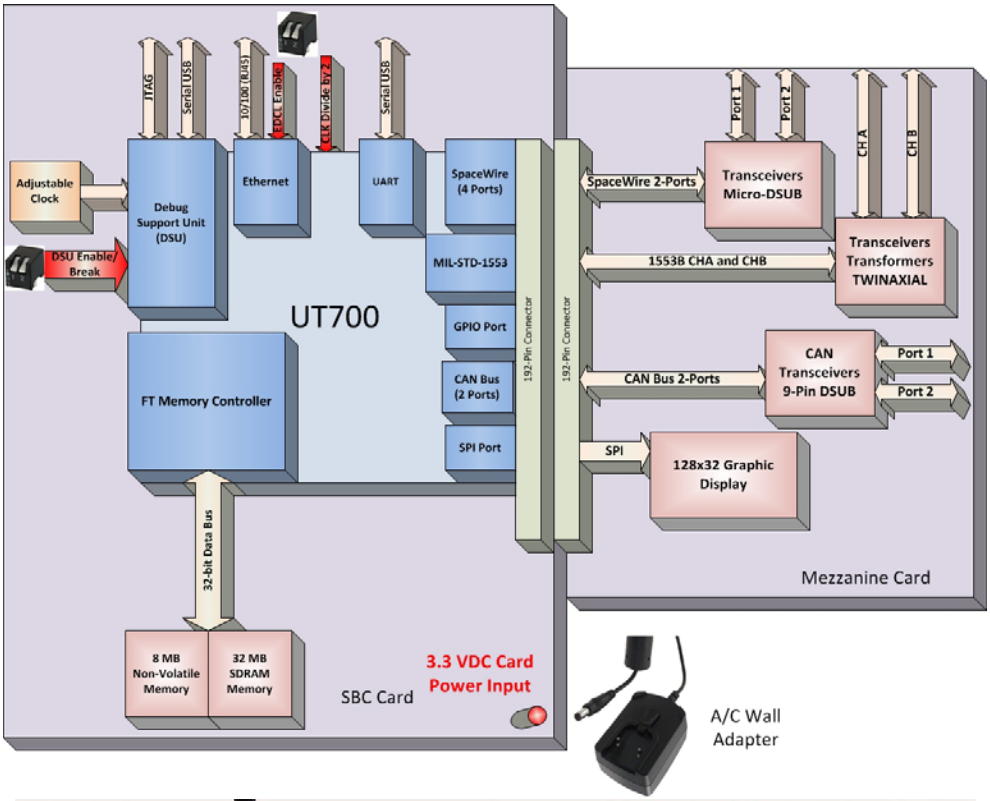
- BCC Bare-C LEON Cross-compiler
- RCC RTEMS ERC32/LEON Cross-compiler system

1.2 Aeroflex LEAP Overview

The Aeroflex LEAP provides a flexible development platform for customers wanting to develop software that works on the Aeroflex UT700 Standard Product with minimal cost investment. The Aeroflex LEAP has the following features:

- An Aeroflex UT700 LEON 3 FT standard product
- 8 Mbytes NV memory storage
- 32Mbytes SDRAM
- One USB UART interface via standard USB
- One 10T/100 Mbit/s Ethernet port
- JTAG interface for programming and debug of UT700 LEON 3FT (requires XILINX USB Platform Cable)
- One 192-pin mezzanine card expansion connector
- On-board Programmable LEAP main clock

A block diagram of the LEAP card is shown in Figure 1.



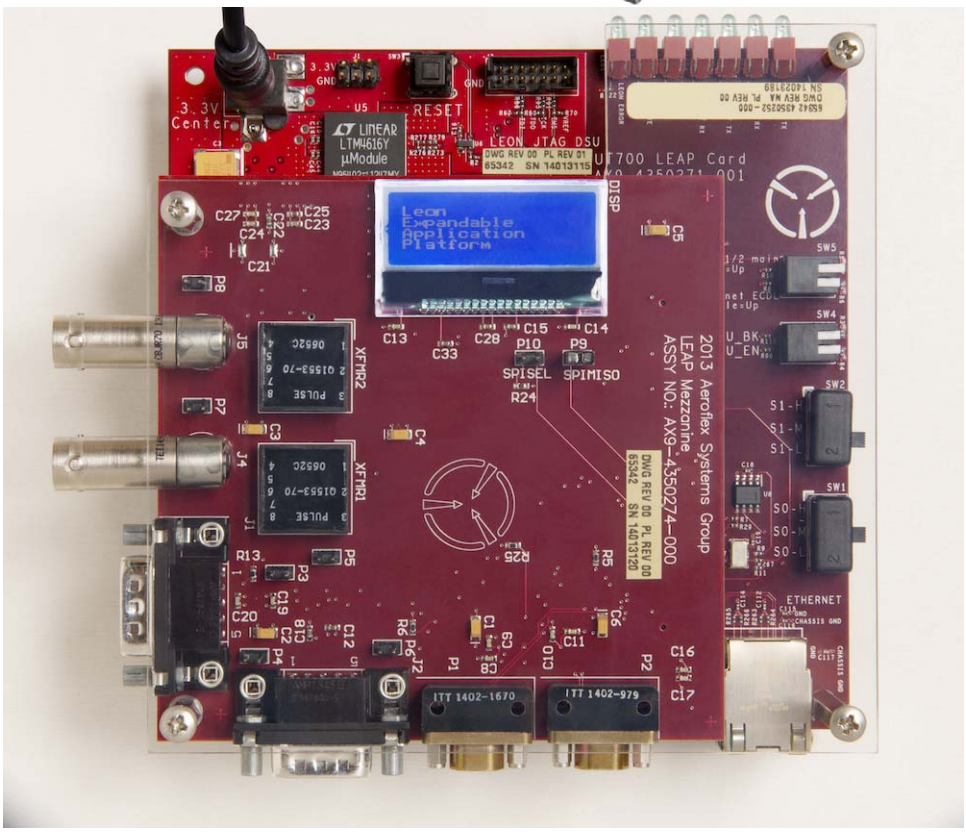


Figure 1: LEAP Top-Level Block Diagram and Assembly (AX9-4250252)

1.3 UT700-LEAP Board Stack Package Contents (Main SBC Only)

- One LEAP card (main SBC & Memory)
- One A/C Wall Adapter
- One Euro-style A/C interface plate
- One US-style A/C interface plate
- One LEAP Board User Guide (CD)

1.4 UT700-LEAP-MEZ Board Stack Package Contents (Main SBC and Mezzanine)

- One LEAP card (main SBC & Memory)
- One LEAP card (mezzanine with SPI display, two CAN bus, two SpaceWire and a dual-redundant CHA/CHB 1553B ports)
- One A/C Wall Adapter
- One Euro-style A/C interface plate
- One US-style A/C interface plate
- One LEAP Board User Guide (CD)

1.5 Aeroflex LEAP Board Power Input

The Aeroflex LEAP utilizes one AC wall-adapter to provide the 3.3VDC used to operate the board. Aeroflex includes the A/C wall adapter in the delivery package to enable “out-of-the-box” software operation and development. Connect the A/C wall adapter DC port-side cable to the LEAP card as shown in Figure , the wall-adapter side should be connected to a compatible A/C wall outlet.

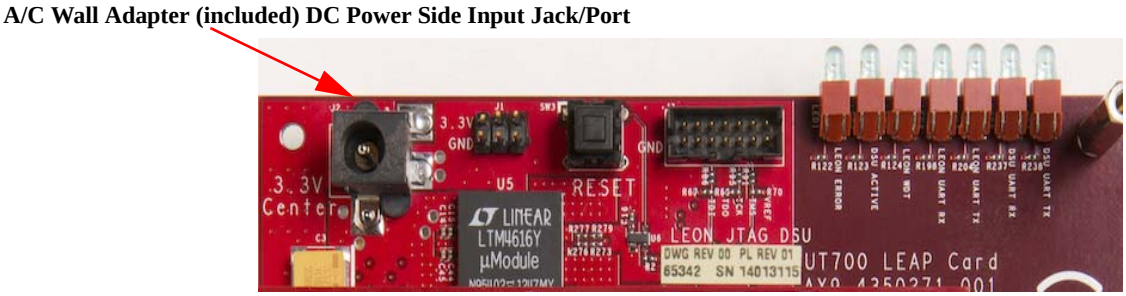


Figure 2: LEAP Power Input

1.6 Reference documents

- N/A

2.0 Architecture

2.1 UT700 Brief Overview

The Aeroflex LEAP design consists of the UT700 Leon 3FTprocessor and a set of IP cores connected through the AMBA AHB/APB buses.

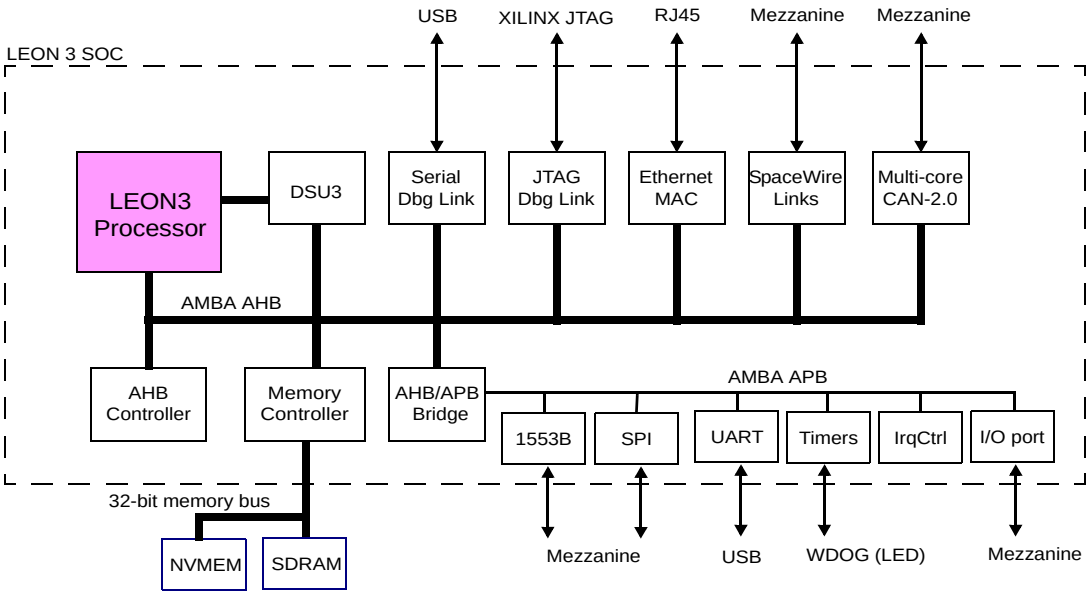


Figure 3: UT700 LEAP Block Diagram

The design is centered around the AMBA Advanced High-Speed bus (AHB), to which the LEON 3 processor and other high-bandwidth devices are connected. External memory is accessed through a combined PROM/SDRAM memory controller. The on-chip peripheral devices include four SpaceWire links, one Ethernet 10/100 Mbit MAC, dual CAN-2.0 interface, one SPI interface, a dual channel 1553B interface, serial and JTAG debug interfaces, a UART, interrupt controller, timers and a 16-bit general purpose I/O port.

2.2 UT700 LEON 3 SPARC V8 Processor

The LEAP's UT700 design is based the LEON 3 SPARC V8 processor. The processor core is configured with a cache system consisting of 4Kbyte, 4-way set associative Instruction and 4Kbyte, 4-way Data cache. The LEON3 debug support unit (DSU3) is a user port for downloading and debugging of programs through the serial or JTAG ports.

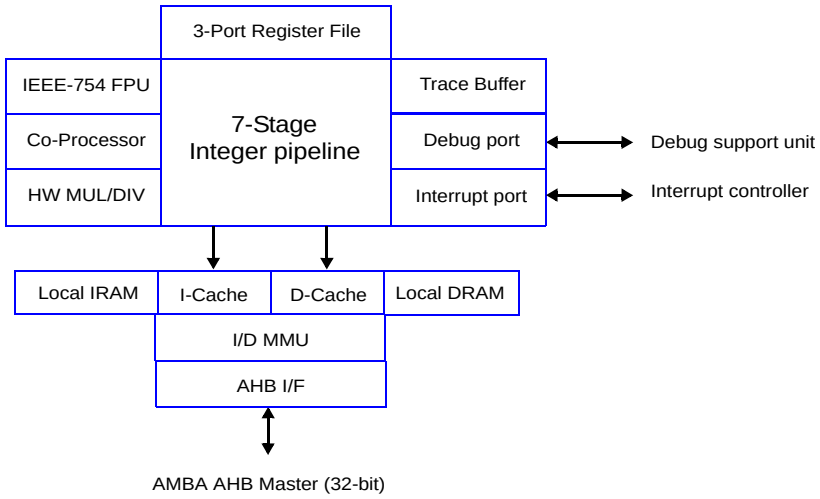


Figure 4: LEON 3 processor core block diagram

2.3 Memory interfaces

The external memory is interfaced through a combined PROM/SDRAM memory controller core (UT700). The Aeroflex LEAP card provides 8 MB of Non-Volatile memory, and 32 MB of SDRAM for system program/data memory.

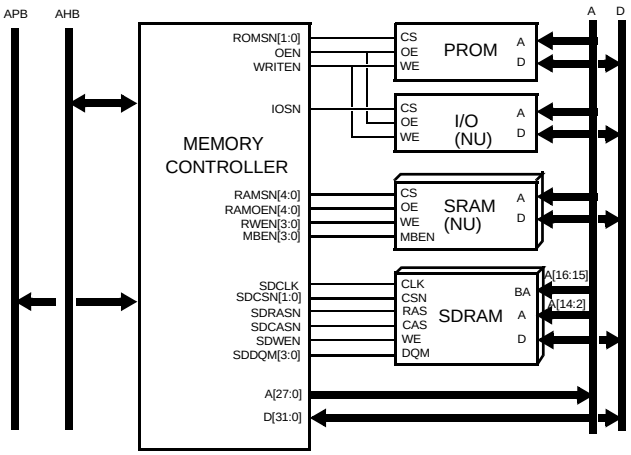


Figure 5: PROM/SDRAM Memory I/F

2.4 SpaceWire links

The LEAP design is configured with four SpaceWire links. Each link is controlled separately through the APB bus, and transfers received and transmitted data through DMA transfer on AHB. All four of the SpaceWire links can be configured with RMAP support and each of the four SpaceWire Ports are routed to the mezzanine connector.

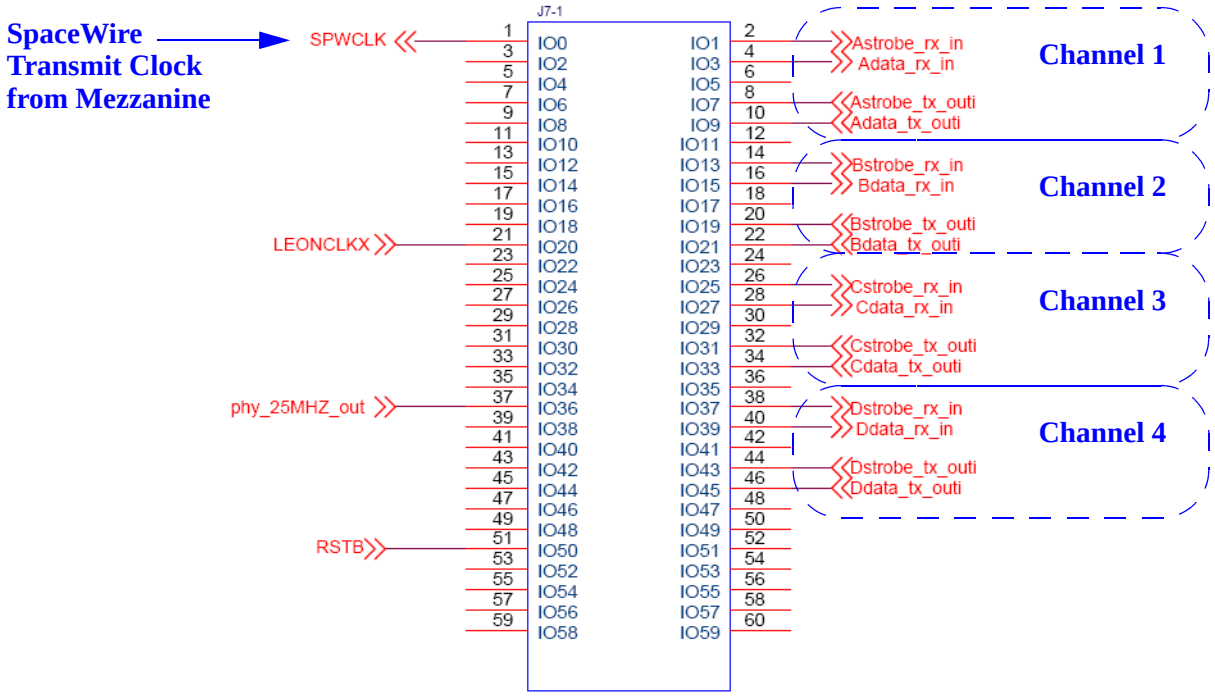


Figure 6: SpaceWire Mezzanine I/F Pinout

2.5 UT700 Timer Unit

The timer unit consists of a common scaler and up to four individual timers. The timers can work in periodical or one-shot mode. If configured to do so, Timer 4 also operates as a watchdog timer, driving the watchdog output signal (WDOG) when expired. The WDOG output signal is connected to a LED (see Figure) and will illuminate if Timer 4 is configured as the WDOG timer and expires.

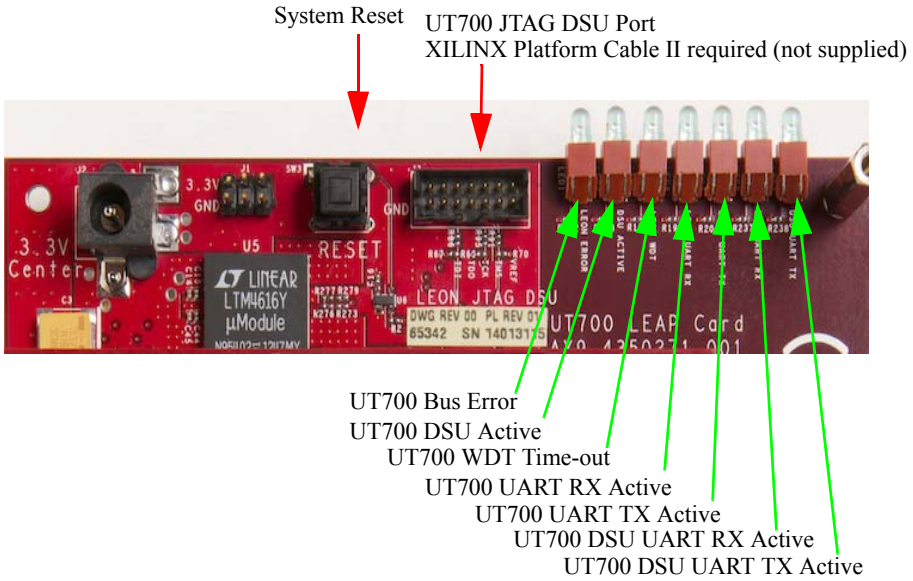

System Reset
UT700 JTAG DSU Port
XILINX Platform Cable II required (not supplied)
UT700 Bus Error
UT700 DSU Active
UT700 WDT Time-out
UT700 UART RX Active
UT700 UART TX Active
UT700 DSU UART RX Active
UT700 DSU UART TX Active

Figure 7: LEAP Reset & LED Indicators

2.6 System Reset Button

A method to generate a manual system-level reset to the LEAP card is provided through a momentary push-button switch (see Figure). The user can issue a system reset to the LEAP card through a simple press-and-release action on the System Reset switch.

2.7 System Status LED Indicators

Several LED's are provided as a visual confirmation/detection of different LEAP card board status conditions (see Figure).

- The most basic of the indicators are the DSU and UART TX/RX LED's. The user should see these LEDs pulse on & off when transfers are occurring on the serial DSU or serial UART USB ports.
- The DSU Active LED is connected to the UT700's DSU Active output pin & will illuminate when the UT700 detects the DSU Enable switch is in the active (down position) and confirms it has enabled the internal DSU.

2.8 USB General Purpose UART I/F

The internal LEON UART is connected to a standard mini USB connector through a standard USB bus transceiver. The UART can be used as a general purpose serial I/O port (see Figure)

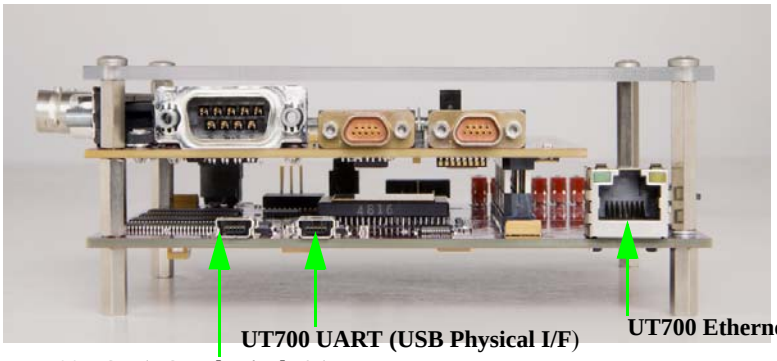


Figure 8: USB and Ethernet I/F

2.9 UT700 Ethernet I/F

The internal LEON Ethernet I/F (10/100) is connected to a standard RJ45 connector through a standard Ethernet bus transceiver. The Ethernet port can be used as a general purpose I/O port (see Figure). An additional feature of the UT700 Ethernet MAC is the built-in EDCL (Ethernet Debug Communication Link) protocol. The user can enable/disable the EDCL function by placing the piano switch down (enable) or up (disable), see Figure 9.

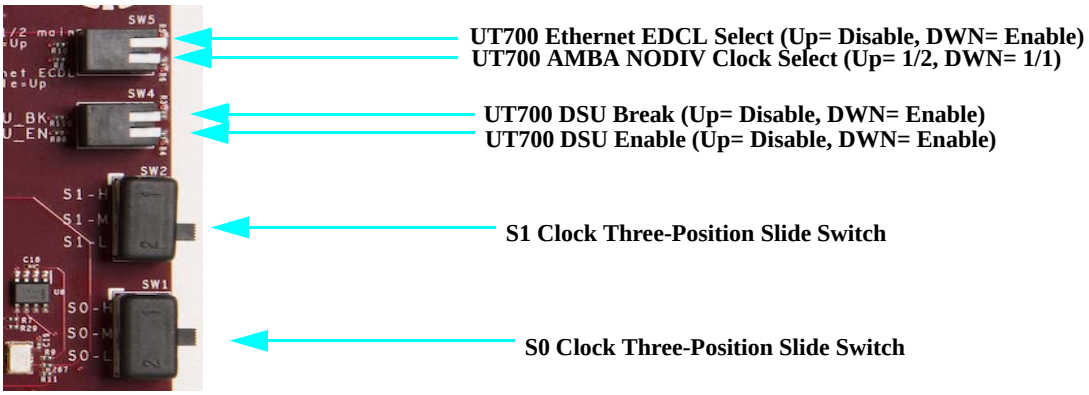


Figure 9: UT700 Mode & System Clock Adjust Selection

2.10 System Clock Selection

Two switches (S0 and S1) control the main clock frequency input to the UT700 (see Figure 9). For this application, the maximum operating clock that can be selected for the UT700 with the AMBA NODIV piano switch (see Figure 9) set to the down (1/1) position is 133MHz. The positions listed in Table 1 outline the valid S0 and S1 position combinations and corresponding UT700 AMBA frequencies.

Table 1:

S1 Position	S0 Position	NODIV	AMBA Frequency
H	M	Up/Down	37.5MHz/75MHz
M	H	Up/Down	41.67MHz/83.33MHz
L	H	Up/Down	62.5MHz/125MHz
L	M	Up/Down	66.65MHz/133.3MHz
H	L	Up/Down	75MHz/Not Valid

2.11 UT700 General Purpose I/O

A general purpose I/O port (GPIO) is provided in the design. The port is 16-bits wide and each bit can be dynamically configured as input or output. The GPIO can also generate interrupts from external devices. The 16-bit GPIO port is connected to the mezzanine connector enabling the user to define the function & interface controlling each pin. See Figure 10.

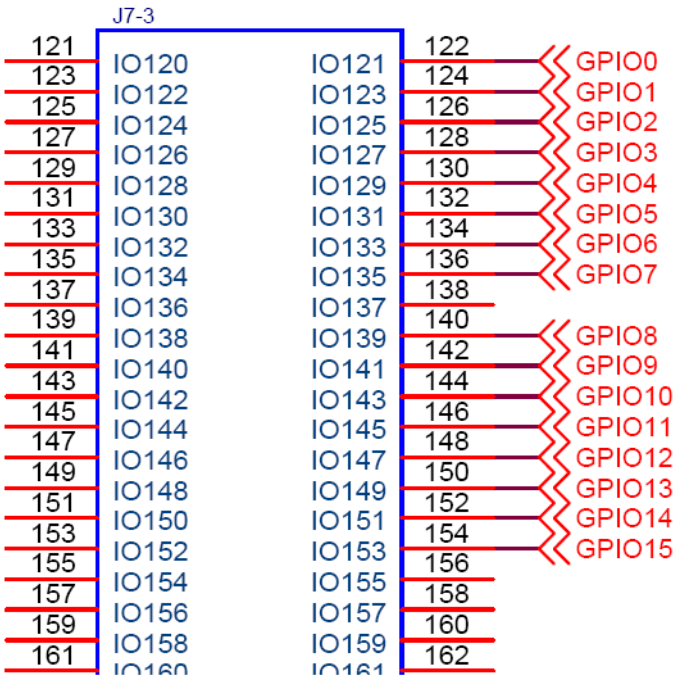


Figure 10: UT700 GPIO I/F to Mezzanine Connector

2.12 UT700 1553B Port to Mezzanine

The UT700's dual-redundant (Channel A & B) 1553B interface is routed to the J7 mezzanine connector as shown in Figure 11. **Note:** the 1553 Clock pin from the mezzanine is a 3.3V logic level input to the UT700 and should be a 20MHz 50% duty-cycle clock if the 1553B port is to be implemented (see UT700 datasheet for details).

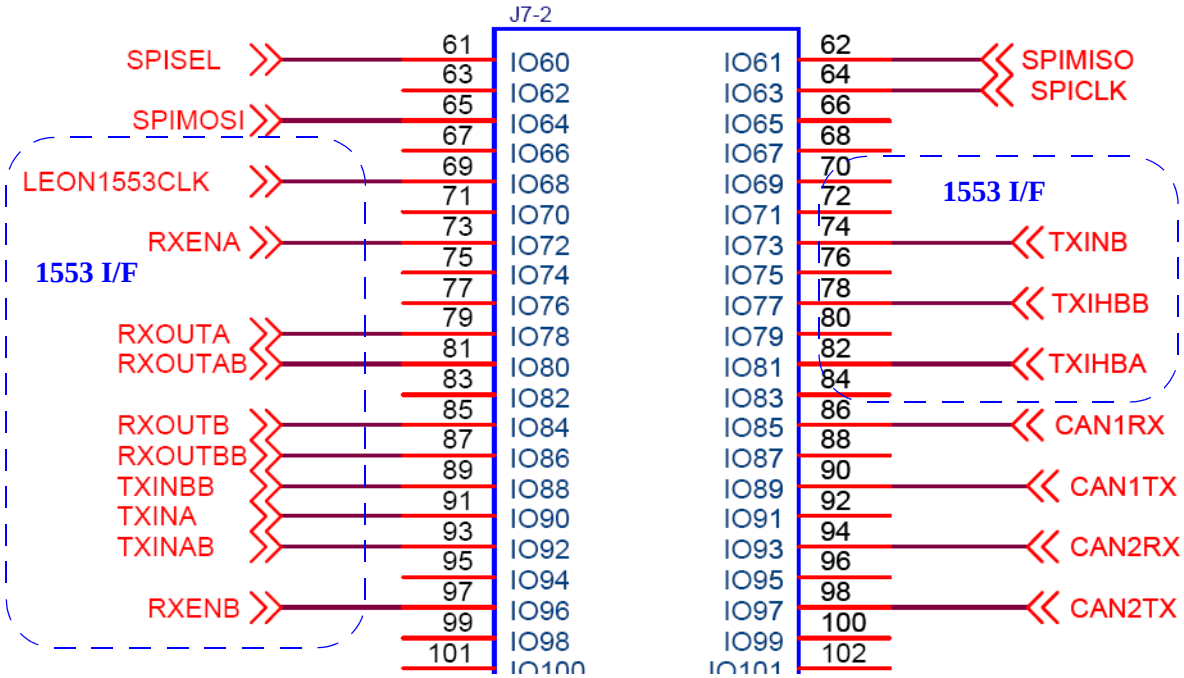


Figure 11: UT700 1553 I/F to Mezzanine Connector

2.13 UT700 CAN Bus Interface

Two CAN-2.0 interfaces are available through the mezzanine interface connector J7. The voltage levels are standard 3.3VDC single-ended signal type. See Figure 12.

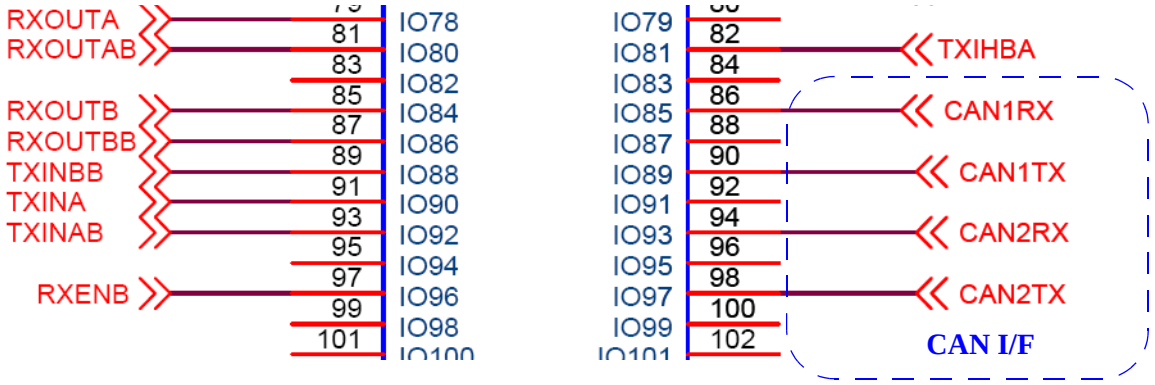


Figure 12: UT700 CAN Bus I/F to Mezzanine Connector

2.14 UT700 SPI Bus Interface

The UT700 SPI bus is routed to the mezzanine connector J7 as shown in Figure 13. The voltage levels used by the SPI interface are standard 3.3VDC single-ended signal type.

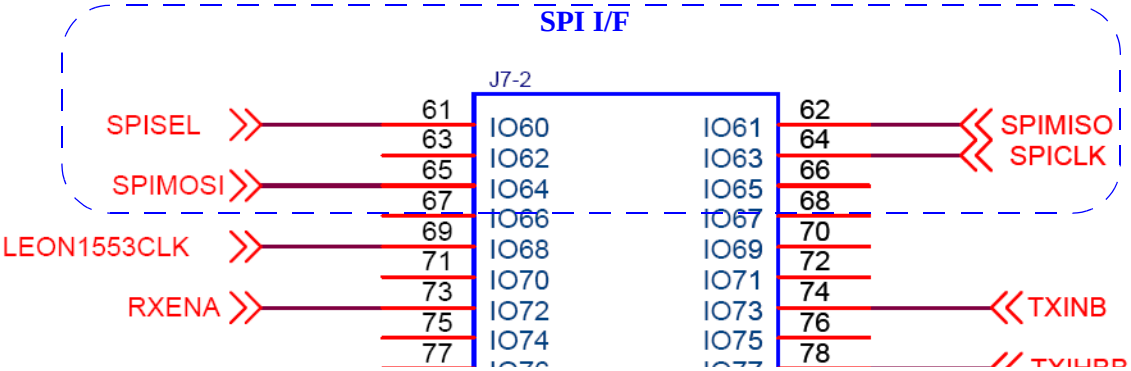


Figure 13: UT700 SPI Bus I/F to Mezzanine Connector

2.15 LEAP Cores

The Aeroflex UT700 SBC design is comprised of various core elements. Figure 14 the initial screen-shot and core listing from a GRMON2 debug session invoked on the LEAP card through the JTAG DSU.

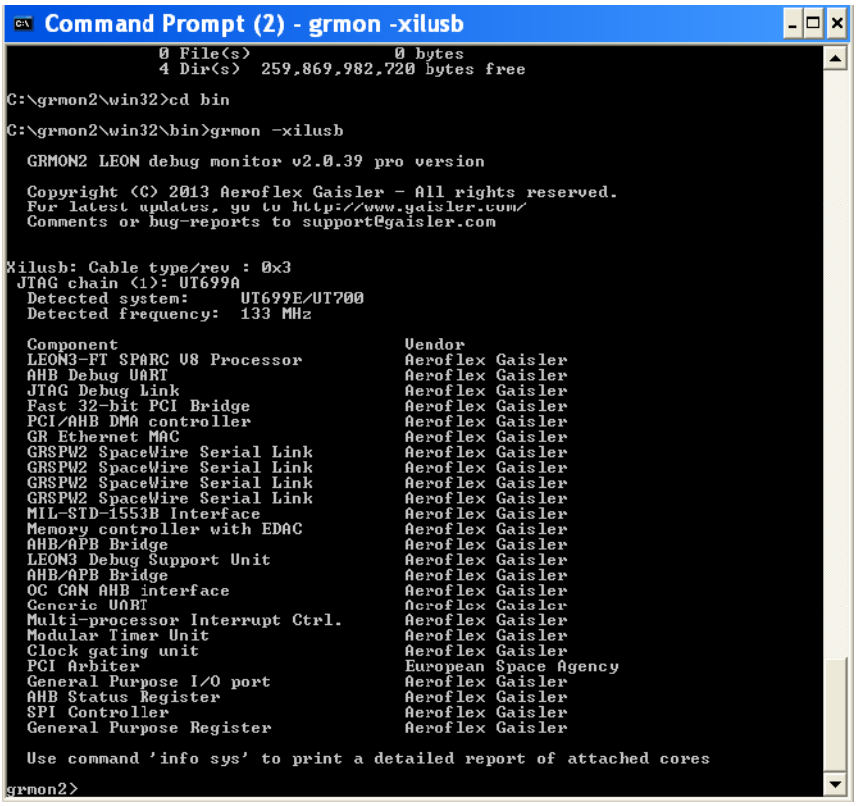

Command Prompt (2) - grmon -xilusb
0 File(s) 0 bytes
4 Dir(s) 259,869,982,720 bytes free
C:\grmon2\win32>cd bin
C:\grmon2\win32\bin>grmon -xilusb
GRMON2 LEON debug monitor v2.0.39 pro version
Copyright (C) 2013 Aeroflex Gaisler - All rights reserved.
For latest updates, go to http://www.gaisler.com/
Comments or bug-reports to support@gaisler.com
Xilusb: Cable type/rev : 0x3
JTAG chain (1): UT699A
Detected system: UT699E/UT700
Detected frequency: 133 MHz
Component Vendor
LEON3-FT SPARC V8 Processor Aeroflex Gaisler
AHB Debug UART Aeroflex Gaisler
JTAG Debug Link Aeroflex Gaisler
Fast 32-bit PCI Bridge Aeroflex Gaisler
PCI/AHB DMA controller Aeroflex Gaisler
GR Ethernet MAC Aeroflex Gaisler
GRSPW2 SpaceWire Serial Link Aeroflex Gaisler
GRSPW2 SpaceWire Serial Link Aeroflex Gaisler
GRSPW2 SpaceWire Serial Link Aeroflex Gaisler
GRSPW2 SpaceWire Serial Link Aeroflex Gaisler
MIL-STD-1553B Interface Aeroflex Gaisler
Memory controller with EDAC Aeroflex Gaisler
AHB/APB Bridge Aeroflex Gaisler
LEON3 Debug Support Unit Aeroflex Gaisler
AHB/APB Bridge Aeroflex Gaisler
OC CAN AHB interface Aeroflex Gaisler
Generic UART Aeroflex Gaisler
Multi-processor Interrupt Ctrl. Aeroflex Gaisler
Modular Timer Unit Aeroflex Gaisler
Clock gating unit Aeroflex Gaisler
PCI Arbiter European Space Agency
General Purpose I/O port Aeroflex Gaisler
AHB Status Register Aeroflex Gaisler
SPI Controller Aeroflex Gaisler
General Purpose Register Aeroflex Gaisler
Use command 'info sys' to print a detailed report of attached cores
grmon2>

Figure 14: LEAP UT700 Core List

2.16 AHB Core Mapping

Once GRMON is online and the screen above displayed in the DOS window, typing the "info sys" command provides the AHB map and associated interrupt assignments of the UT700's core elements. An example system information screen is shown in Figure 15.

cpu0 Aeroflex Gaisler LEON3-FT SPARC V8 Processor
AHB Master 0
ahbuart0 Aeroflex Gaisler AHB Debug UART
AHB Master 1
APB: 80000700 - 80000800
Baudrate 115200, AHB frequency 133.00 MHz
ahbjtag0 Aeroflex Gaisler JTAG Debug Link
AHB Master 2
pci0 Aeroflex Gaisler Fast 32-bit PCI Bridge
AHB Master 3
AHB: C0000000 - 00000000
AHB: FFF00000 - FFF20000
APB: 80000400 - 80000500
IRQ: 3
adev4 Aeroflex Gaisler PCI/AHB DMA controller
AHB Master 4
APB: 80000500 - 80000600
greth0 Aeroflex Gaisler GR Ethernet MAC
AHB Master 5
APB: 80000E00 - 80000F00
IRQ: 14
edcl ip 192.168.0.64, buffer 2 kbyte
grspw0 Aeroflex Gaisler GRSPW2 SpaceWire Serial Link
AHB Master 6
APB: 80000A00 - 80000B00
IRQ: 10
Number of ports: 1
grspw1 Aeroflex Gaisler GRSPW2 SpaceWire Serial Link
AHB Master 7
APB: 80000B00 - 80000C00
IRQ: 11
Number of ports: 1
grspw2 Aeroflex Gaisler GRSPW2 SpaceWire Serial Link
AHB Master 8
APB: 80000C00 - 80000D00
IRQ: 12
Number of ports: 1
grspw3 Aeroflex Gaisler GRSPW2 SpaceWire Serial Link
AHB Master 9
APB: 80000D00 - 80000E00
IRQ: 13
Number of ports: 1
gr1553b0 Aeroflex Gaisler MIL-STD-1553B Interface
AHB Master 10
APB: 80100000 - 80100100
IRQ: 17
features: BC RT BM, codec clock: 20 MHz
Device index: 0
mctrl0 Aeroflex Gaisler Memory controller with EDAC
AHB: 00000000 - 20000000
AHB: 20000000 - 40000000
AHB: 40000000 - 80000000
APB: 80000000 - 80000100
32-bit prom @ 0x00000000
32-bit sdram: 1 * 32 Mbyte @ 0x40000000
col 9, cas 3, ref 7.8 us
apbmst0 Aeroflex Gaisler AHB/APB Bridge
AHB: 80000000 - 80100000
dsu0 Aeroflex Gaisler LEON3 Debug Support Unit
AHB: 90000000 - A0000000
AHB trace: 256 lines, 32-bit bus
CPU0: win 8, hwbp 2, itrace 256, V8 mul/div, srmmu, lddel 1, GRFPU
stack pointer 0x41fffff0
icache 4 * 4 kB, 32 B/line lru
dcache 4 * 4 kB, 16 B/line lru
apbmst1 Aeroflex Gaisler AHB/APB Bridge
AHB: 80100000 - 80200000
occan0 Aeroflex Gaisler OC CAN AHB interface
AHB: FFF20000 - FFF21000
IRQ: 4
cores: 2
uart0 Aeroflex Gaisler Generic UART
APB: 80000100 - 80000200
IRQ: 2
Baudrate 38394
irqmp0 Aeroflex Gaisler Multi-processor Interrupt Ctrl.
APB: 80000200 - 80000300
EIRQ: 9
gptimer0 Aeroflex Gaisler Modular Timer Unit
APB: 80000300 - 80000400
IRQ: 6
12-bit scalar, 4 * 32-bit timers, divisor 133
grcg0 Aeroflex Gaisler Clock gating unit
APB: 80000600 - 80000700
GRMON did NOT enable clocks during initialization
adev20 European Space Agency PCI Arbiter
APB: 80000800 - 80000900
gpio0 Aeroflex Gaisler General Purpose I/O port
APB: 80000900 - 80000A00
ahbstat0 Aeroflex Gaisler AHB Status Register
APB: 80000F00 - 80001000
IRQ: 1
spi0 Aeroflex Gaisler SPI Controller
APB: 80100100 - 80100200
IRQ: 18
FIFO depth: 16, 1 slave select signals
Maximum word length: 32 bits
Controller index for use in GRMON: 0
grgpreg0 Aeroflex Gaisler General Purpose Register
APB: 80100200 - 80100300

Figure 15: LEAP UT700 Core Information List

2.17 Non-Volatile Memory Mapping

The LEAP card offers the user access to 8Mbytes of contiguous Non-Volatile (NV) memory storage. The base address for the 32-bit wide PROM space is 0x00000000. The user has the ability to write data into the NV memory by setting the PROM write enable bit in the UT700 memory configuration register (see UT700 Datasheet for details).

2.18 SDRAM Memory Mapping

The LEAP card offers the user access to 32Mbytes of contiguous volatile memory storage. The base address for the 32-bit wide SDRAM space is 0x40000000; all programs targeting the LEAP card should compile programs using this base address.

3.0 Mezzanine Power Interface

3.1 Mezzanine Connector Power

The LEAP card supplies 3.3 VDC (0.75A max) and 2.5 VDC (0.5A max) to the mezzanine connector; each supply shares common ground (GND) pins. The mezzanine power connector map/pin-out is shown in Figure 16.

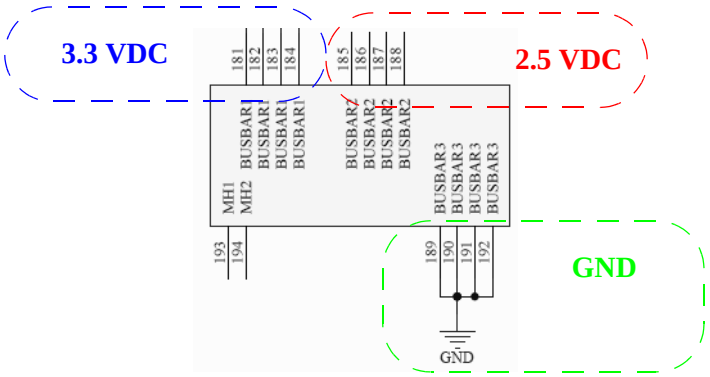


Figure 16: LEAP Power I/F to Mezzanine

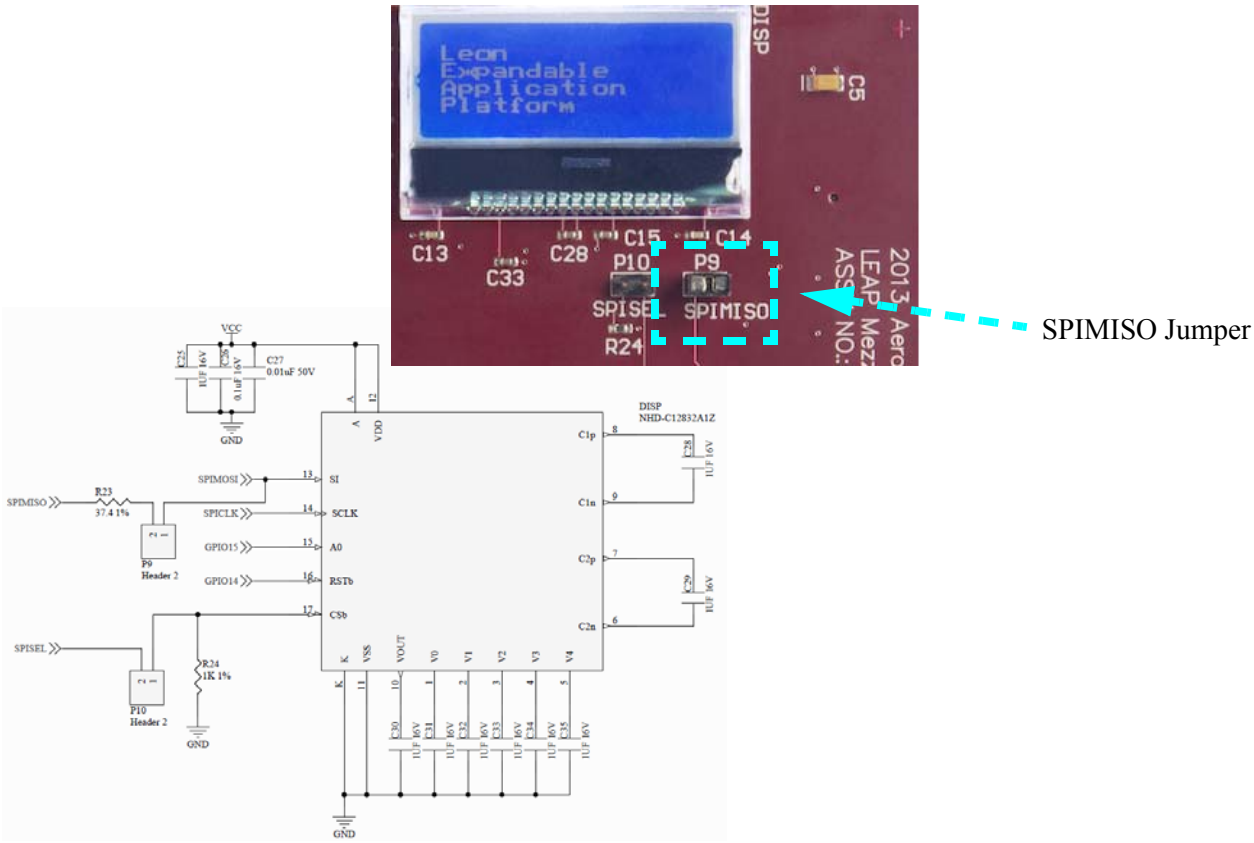
4.0 Optional LEAP with Mezzanine Card

4.1 Mezzanine Card SPI Interface

The LEAP SBC card routes the UT700 SPI interface signals to the mezzanine connector. The mezzanine card incorporates a 128x32 LCD Display (New Haven Display PN NHD-C12832A1Z-NSW-BBW-3V3. Since the LCD display does not have a SPI output port (input mode only), a jumper (P9) on the mezzanine can be used to loop-back the data sent by the UT700 SPI port to the display. When the P9 Jumper is installed, the SPI data sent will be seen in the SPI data RX register.

Additionally, the LCD display requires two additional inputs for reset and A0 (command/data). The UT700 GPIO[15] is connected to the LCD A0 input; the UT700 GPIO[14] is connected to the LCD reset input. **Note:** both GPIO[15:14] are pulled-low via 10K ohm resistors on the SBC card to hold the display in reset and A0 to a known state after power is applied to the system.

The New Haven Display Data Sheet contains additional information for the initialization and use of the graphic display.



4.2 Mezzanine Card CAN Bus 1 Interface

The LEAP SBC card routes the UT700 CAN bus 1 and 2 interface signals to the mezzanine connector. The mezzanine card incorporates the CAN transceivers and standard 9-pin Dsub connectors along with the 120 ohm end-bus termination resistor. For CAN Bus 1, refer to Figure 17. The 120 ohm termination resistor can be installed (jumper on P3) or open (jumper on P3 not installed). The optional ground connection to pin 5 of the Dsub connector can be selected by installing a block jumper on P4 as shown in Figure 17.

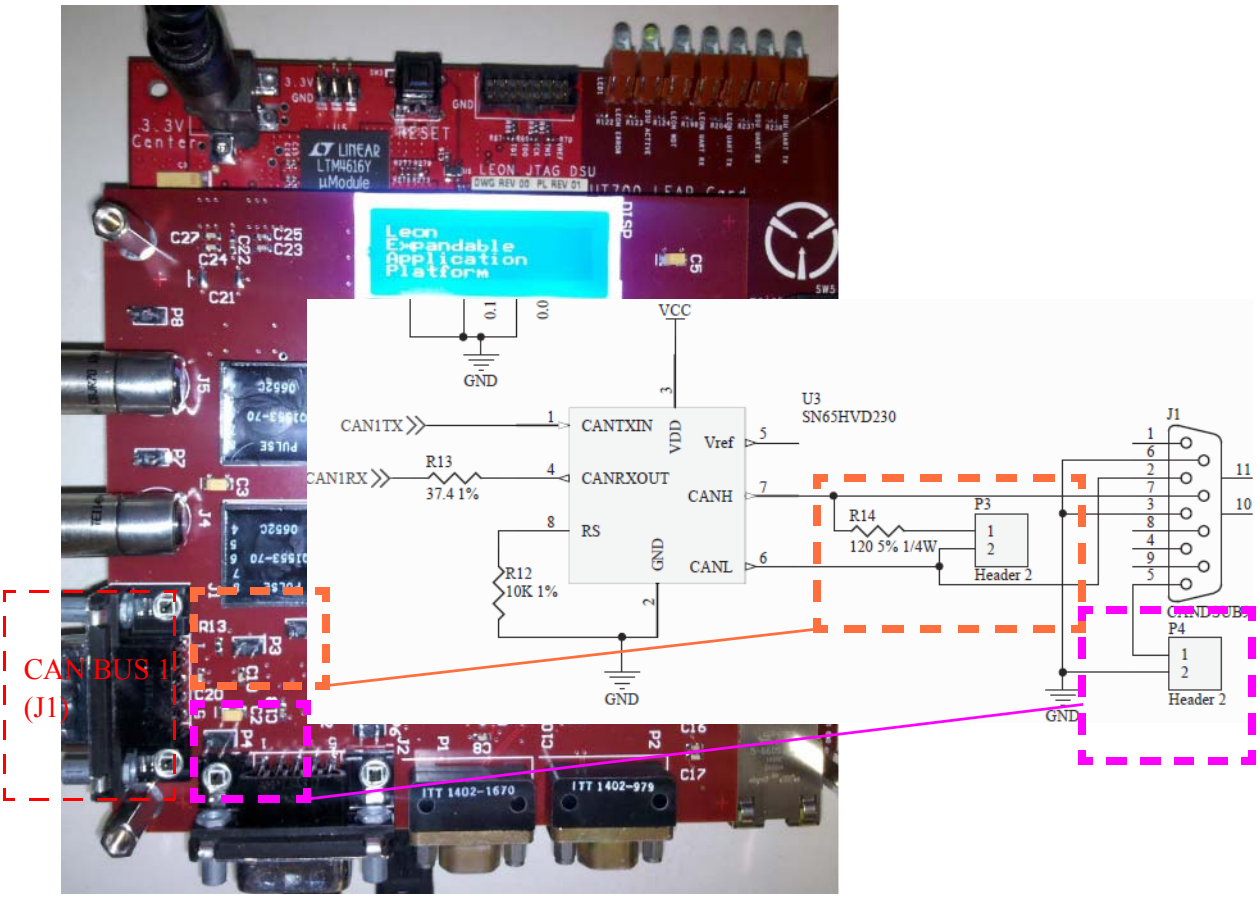


Figure 17: CAN Bus 1 I/F

4.3 Mezzanine Card CAN 2 Bus Interface

The LEAP SBC card routes the UT700 CAN bus 1 and 2 interface signals to the mezzanine connector. The mezzanine card incorporates the CAN transceivers and standard 9-pin Dsub connectors along with the 120 ohm end-bus termination resistor. For CAN Bus 2, refer to Figure 18. The 120 ohm termination resistor can be installed (jumper on P5) or open (jumper on P5 not installed). The optional ground connection to pin 5 of the Dsub connector can be selected by installing a block jumper on P6 as shown in Figure 18.

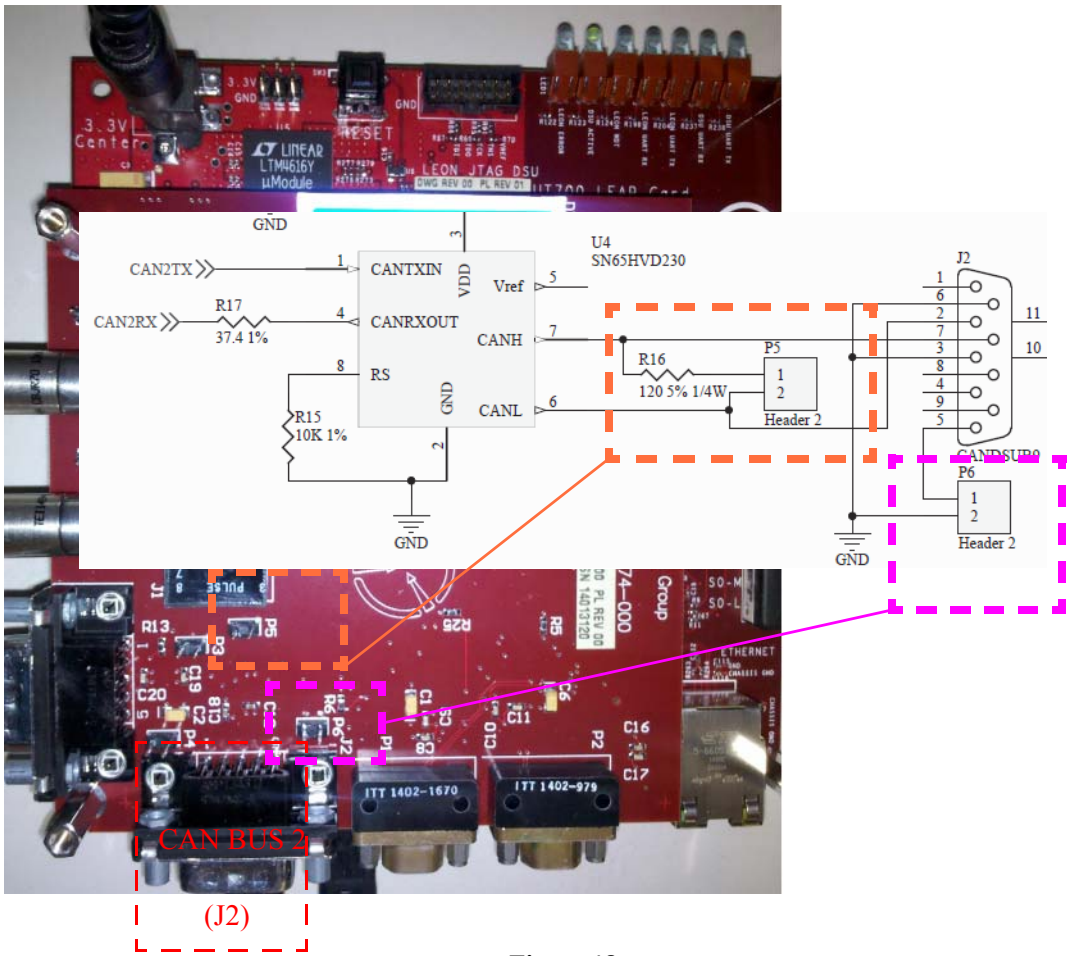


Figure 18: CAN Bus 2 I/F

4.4 Mezzanine Card 1553B Interface

The LEAP SBC card routes the UT700 1553B interface signals to the mezzanine connector. The mezzanine card incorporates a standard set of 1553B bus transceiver and transformers. For 1553B bus connector orientation, refer to Figure 19. The optional ground connection to the shield of the 1553B bus connector can be selected by installing a block jumper on P7 for CHA and P8 for CHB as shown in Figure 19.

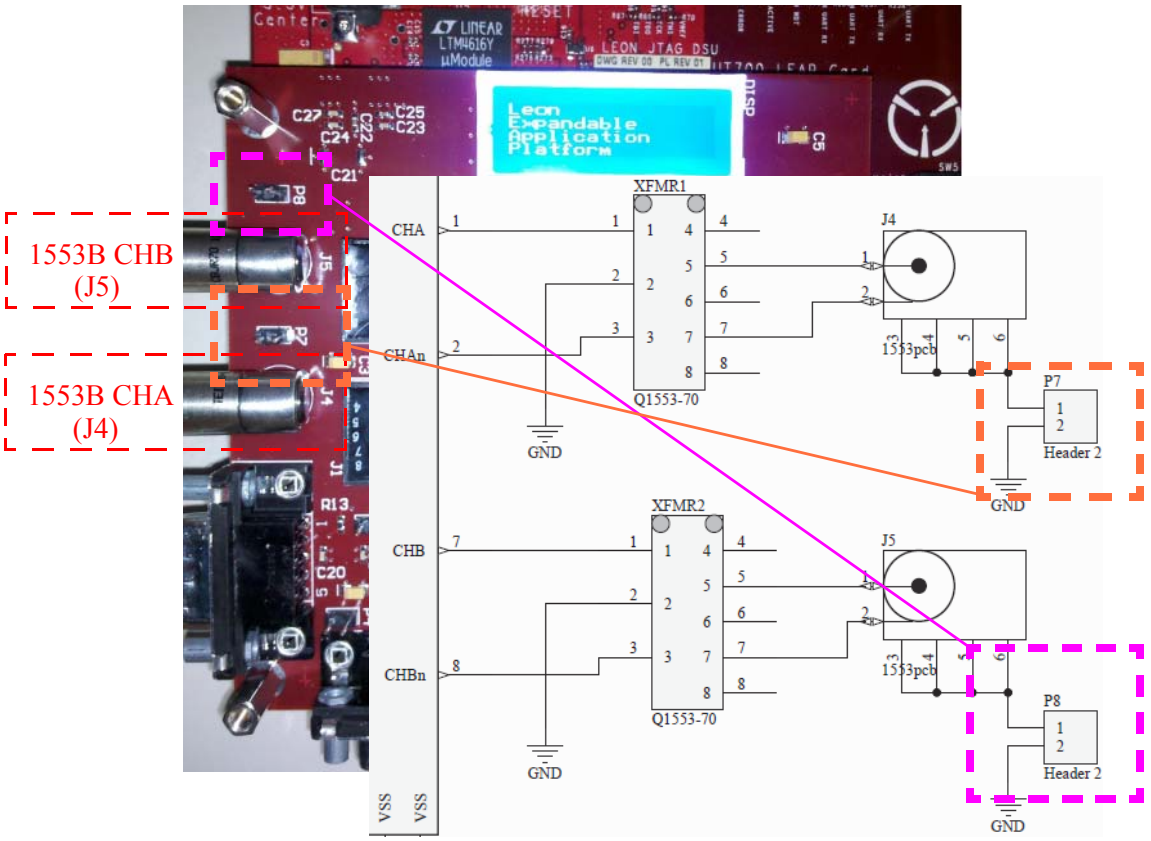


Figure 19: 1553 Bus I//F

4.5 Mezzanine Card SpaceWire Interface

The LEAP SBC card routes the UT700 SpaceWire interface signals to the mezzanine connector. The mezzanine card incorporates a standard set of SpaceWire transmitter/receiver interface devices ported to the 9-pin micro-D SpaceWire connectors. The SpaceWire bus connector orientation is shown in Figure 20. Only two of the four SpaceWire channels are provided on the mezzanine card. These channels are Port 0 (P1) and Port 1 (P2) of the UT700.

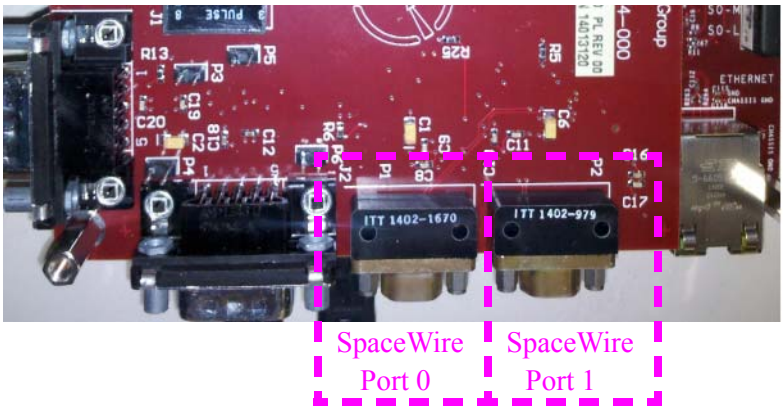


Figure 20: SpaceWire Bus I//F

4.6 Option for Mezzanine Card Purchase

If a customer currently has one main card (UT700-LEAP) and later wants the plugin mezzanine card (UT700-MEZ), Aeroflex does offer the standalone plugin mezzanine card for purchase. **NOTE:** The UT700-MEZ card cannot operate standalone. It does require the main card.

Table 2. Order Information

UT Part Number	Description
UT700-LEAP-MEZ	UT700 LEAP w/MEZ
UT700-LEAP	UT700 LEAP only, no MEZ
UT700-MEZ	UT700 MEZ card only

5.0 Software development

5.1 Tool chains

The LEON3 processor is supported by several software tool chains:

- Bare-C cross-compiler system (BCC)
- RTEMS cross-compiler system (RCC)
- Snapgear embedded linux
- eCos real-time kernel
- VxWorks 6.5 /6.7
- ThreadX
- Nucleus

All these tool chains and associated documentation can be obtained from www.gaisler.com.

5.2 Downloading software to the target system

LEON3 has an on-chip debug support unit (DSU) which greatly simplifies the debugging of software on a target system. The DSU provides full access to all processor registers and system memory and also includes instruction and data trace buffers. Downloading and debugging of software is done using the GRMON debug monitor, a tool that runs on the host computer and communicates with the target through either serial or JTAG interfaces.

Please refer to the GRMON User's Manual for a description of the GRMON operations at www.gaisler.com.

5.3 RTEMS demo

The RTEMS tool chain (RCC) contains a driver for the spacewire core in the LEON3 SOC design. The operation of the driver is described in the RTEMS SPARC BSP Manual. A sample SpaceWire application is provided with the SOC design in software/rtems-shell.

5.4 VxWorks

The VxWorks BSP contains a set of drivers for the spacewire core in the LEON3 SOC design. The operation of the driver is described in the VxWorks-drivers manual. The supported hardware is summarized in the list below. For documentation about a specific core's driver please see the LEON VxWorks 6.7 Driver Manual.

• LEON3

• MMU

• FPU, hardware MUL/DIV and software MUL/DIV support

• Interrupt controller

• UART console/terminal driver

• Timer unit

• General Purpose I/O (GRGPIO)

• 10/100 Ethernet networking (GRETH)

• SpaceWire (GRSPW)

• Non-DMA CAN 2.0 (OCCAN)

5.5 Linux Support

LINUX support for the LEON3 is provided through a special version of the SnapGear Embedded Linux distribution. SnapGear Linux is a full source package, containing kernel, libraries and application code for rapid development of embedded Linux systems. The LEON port of SnapGear on the LEAP systems supports the MMU configuration, V8 mul/div instructions and the floating-point unit (FPU). The version of the Linux kernel being used is µCLinux 2.6.21. Below is a list of supported hardware:

- LEON3, with MMU, FPU, MUL/DIV.
- Non-standard page size, larger that 4KBytes
- APBUART
- GPTIMER
- GRETH 10/100 and Gbit

The Linux Kernel is loaded into the LEAP Non-Volatile memory (address 0x00000000) via GRMON. Once the Kernel load is complete, the user may press and release the reset button to initiate a Kernel transfer into SDRAM. To view the kernel boot window, connect to the UART mini-USB Port on LEAP to a PC with a communication terminal window running at 38400 BAUD. Example Linux boot Screen

Once loaded via GRMON, the LEAP system boots the Linux kernel. The expected output for the “ls” input command displayed in the terminal window is shown below.

```
io scheduler noop registered
io scheduler cfq registered (default)
grlib apbuart: 1 serial driver(s) at [0x80000100(irq 2)]
grlib apbuart: system frequency: 66000 khz, baud rates: 38400 38400
ttyS0 at MMIO 0x80000100 (irq = 2) is a Leon
Testing fifo size for UART port 0: got 8 bytes.
RAMDISK driver initialized: 16 RAM disks of 4096K size 1024 blocksize
loop: loaded (max 8 devices)
RAMDISK: Compressed image found at block 0
VFS: Mounted root (romfs filesystem) readonly.
Freeing unused kernel memory: 124k freed
init started: BusyBox v1.8.2 (2011-09-27 16:02:09 MDT)
starting pid 14, tty '': '/etc/init.d/rcS'
mount: mounting tmpfs on /var/tmp failed: Invalid argument
ifconfig: socket: Function not implemented
ifconfig: socket: Function not implemented
route: socket: Function not implemented
route: socket: Function not implemented
starting pid 25, tty '': '/bin/sh'
/ # ls
bin      etc      lib      mnt      sbin     tmp      var
dev      home     linuxrc  proc     sys      usr
/ #
```

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